Patent
Attorney's Docket No. F0691

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Patent Application of	)	
	)	
Yatin R. ACHARYA *et al.*	)	Group Art Unit: 2616
	)	
Application No.: 09/816,333	)	Examiner: B. Wong
	)	
Filed: March 26, 2001	)	
	)	
For: SYSTEMS AND METHODS FOR	)	
EXPEDITING THE	)	
IDENTIFICATION OF PRIORITY	)	
INFORMATION FOR RECEIVED	)	
PACKETS	)	

APPEAL BRIEF

U.S. Patent and Trademark Office
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Alexandria, VA 22314

Sir:

This appeal is from the decision of the Primary Examiner dated August 25, 2006 and in support of the Notice of Appeal filed November 27, 2006.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

To the best of the knowledge of the undersigned, there are no other appeals, interferences or judicial proceedings known to the Appellants, the Appellants' legal representative, or the above-noted assignee that will directly affect or be directly affected by, or have a bearing on, the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-4, 8-11 and 13-22 are currently pending in the application. Claims 21 and 22 have been allowed. Claims 8, 13, 18 and 20 have been indicated as being allowable by the Examiner if rewritten in independent form. Claims 1-4, 9-11, 14-17 and 19 were finally rejected in the final Office Action dated August 25, 2006. Claim 15 is the subject of the present appeal.

IV. STATUS OF AMENDMENTS

Appellant has filed herewith, pursuant to 37 C.F.R. § 41.33(b), an amendment that proposes canceling claims 1-4, 9-11, 14 and 16-20 without prejudice or disclaimer and proposes re-writing dependent claims 8, 13, and 15 into independent form. The amendment filed herewith, thus, merely cancels claims or rewrites dependent claims into independent form and, therefore, may be properly entered under 37 C.F.R. § 41.33(b). For purposes of this appeal,

Appellants have assumed that the amendment under 37 C.F.R. § 41.33(b) submitted herewith will be entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 15 recites a multiport network device (180, FIG. 1) that includes a plurality of input ports configured to receive a plurality of data frames, each of the data frames specifying at least one of a plurality of classes of service (205, FIG. 2; pg. 5, lines 15-25; pg. 8, lines 26-31). The device further includes a plurality of output ports configured to transmit at least some of the data frames (210, FIG. 2; pg. 13, lines 19-20) and a plurality of priority queues (240, FIG. 3; pg. 13, lines 13-15) associated with each of the output ports. The device also includes a memory configured to store a plurality of priority levels, one for each of the plurality of classes of service, wherein the memory is configured to be preprogrammed with the plurality of priority levels by a host device (610-640, FIG. 6; pg. 12, lines 15-20). The device additionally includes an action generator (340, FIG. 3; pg. 13, lines 1-6) including: an action memory configured to store a plurality of entries, a decoder configured to identify one of the entries in the action memory for each of the data frames, and a tag generator configured to generate an action tag based on the entry identified for each of the data frames (pg. 13, lines 1-6). The device further includes a port vector queue configured to access the memory to retrieve one of the stored priority levels that corresponds to a class of service specified by each of the data frames using the action tag from

the action generator for the data frame and identify one of the priority queues based on the identified priority level information for the data frame (235, FIG. 2; pg. 13, lines 7-12).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim 15 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 6,798,793 (hereinafter "MA") in view of U.S. Patent Application Publication No. 2002/0118691 (hereinafter "LEFEBVRE").

VII. ARGUMENT

A. The rejection of claim 15 under 35 U.S.C. §103(a) as allegedly being unpatentable over MA in view of LEFEBVRE should be reversed.

In paragraph 5, the final Office Action rejects claim 15 under 35 U.S.C. §103(a) as allegedly being unpatentable over MA in view of LEFEBVRE. Appellants submit that the final Office Action has failed to establish a *prima facie* case of obviousness.

As one requirement for establishing a *prima facie* case of obviousness, the reference (or references when combined) cited by the Office Action must teach or suggest all of the claim features. *In re Vaeck*, 947 F.2d 488, U.S.P.Q.2d 1438 (Fed. Cir. 1991). See M.P.E.P. § 2143. Appellants respectfully submit that the references cited by the final Office Action, either singly

or in combination, do not teach or suggest each and every feature of claim 15.

Claim 15 recites a "multiport network device" that includes "a plurality of input ports configured to receive a plurality of data frames, each of the data frames specifying at least one of a plurality of classes of service," "a plurality of output ports configured to transmit at least some of the data frames," "a plurality of priority queues associated with each of the output ports," "a memory configured to store a plurality of priority levels, one for each of the plurality of classes of service, wherein the memory is configured to be preprogrammed with the plurality of priority levels by a host device," "an action generator including: an action memory configured to store a plurality of entries, a decoder configured to identify one of the entries in the action memory for each of the data frames, and a tag generator configured to generate an action tag based on the entry identified for each of the data frames" and "a port vector queue configured to access the memory to retrieve one of the stored priority levels that corresponds to a class of service specified by each of the data frames using the action tag from the action generator for the data frame and identify one of the priority queues based on the identified priority level information for the data frame."

Appellants submit that MA and LEFEBVRE do not disclose, or even suggest, among other features, "a memory configured to store a plurality of priority levels, one for each of the plurality of classes of service, wherein the memory is configured to be preprogrammed with the plurality of priority levels by a host device" and "a port vector queue configured to access the

memory to retrieve one of the stored priority levels that corresponds to a class of service specified by each of the data frames using the action tag from the action generator for the data frame and identify one of the priority queues based on the identified priority level information for the data frame," as recited in claim 15.

In rejecting claim 15, the final Office Action ("Response to Arguments" section on pg. 2) cites to column 9, lines 29-67; column 11, lines 8-16; and column 11, lines 61-65 of MA for allegedly disclosing "a memory configured to store a plurality of priority levels, one for each of the plurality of classes of service" and "a port vector queue configured to access the memory to retrieve one of the stored priority levels that corresponds to a class of service specified by each of the data frames using the action tag from the action generator for the data frame and identify one of the priority queues based on the identified priority level information for the data frame." On page 6, the final Office Action, though, admits that MA does not disclose a memory that is preprogrammed with the priority level information. The final Office Action (pg. 7), however, cites to paragraph [0043] of LEFEBVRE for allegedly disclosing this feature. Appellants submit that MA and LEFEBVRE, either singly or in combination do not suggest or disclose the combination of features recited in claim 15.

At column 9, lines 29-67, MA discloses:

> Referring to FIG. 7, a router 700 is shown which includes multiple input interfaces 701 each having a respective input interface line or card. Each input interface line may have one or more queued packets waiting to be processed and routed by router 700. Additionally, each queued packet may have a different associated priority level which specifies the particular Quality of Service (QoS)

> level to be used when handling that packet. Each computer network may support a variety of different QoS priority levels, which may include, for example, high priority service for multimedia traffic (e.g., voice and/or video streams), and low priority service for best effort traffic. Further, the best effort traffic may also be subdivided into a plurality of differentiated priority levels within the best-effort class.
>
> When a packet at the input interface is processed by router 700, the packet is first dequeued from the input interface, and is then decapsulated from its data link frame, which is represented in FIG. 7 by decapsulation block 702. After decapsulation, the packet undergoes classification at 704, whereupon the associated priority level of the packet is determined. In case that QoS features are supported (such as, for example, sophistocated queuing, traffic engineering, congestion control, security checking, and/or policy routing), the packet classification may also need to identify a particular flow or traffic class to which the packet belongs. Additionally, other processing events (not shown) may occur before classification such as, for example, checksumming, wherein the number of bytes in the packet is verified before commencing with further processing of the packet. An additional processing event may include access list verification (706). Thereafter, the appropriate output interface for the packet is then determined by a Forwarding Information Base (FIB) look-up (sometimes referred to as Routing Table look-up), as shown at 708. The packet is then encapsulated and routed to its appropriate output interface queue within QoS output queuing structure 710. Typically, each queue (e.g., Q0, Q1, etc.) is a separate FIFO queue representing a distinct priority level of the QoS priority classes.

This section of MA discloses that each packet indicates a priority level that specifies the particular Quality of Service (QoS) level that is to be used when handling the packet. Based on classification of the packet, using the priority level indicated by the packet, the packet is queued in a separate output queue representing that priority level. This section, thus, discloses the storage of a packet, which includes a priority level indicator within the packet, within an output queue corresponding to the priority level.

At column 11, lines 8-16, MA discloses:

> In accordance with the technique of the present invention, a two-phase packet processing technique is provided for processing packets at router 800 (FIG. 8A). During Phase 1, packets are dequeued from the input interface 801 and preprocessed. In a specific embodiment, the preprocessing includes packet decapsulation and classification in order to identify the associated priority level of each processed packet to thereby determine whether or not a particular packet is delay-sensitive.

This section of MA merely discloses the queueing of a received packet at an input interface 801, decapsulation of the received packet, and classification of the packet to identify its associated priority level.

At column 11, lines 61-65, MA discloses:

> The intermediate data structure 814 may be any data structure suitable for storing and retrieving packets. Examples of data structures include an array of queues (FIG. 8B), a linked list, a priority queue, a calendar queue, a binary tree, a binary heap, a FIFO queue, etc.

This section of MA discloses a data structure 814 for storing received packets. The data structure 814 may include a number of different data structures, including an array of queues, a linked list, a priority queue or a binary tree.

Taking the disclosure of column 9, lines 29-67; column 11, lines 8-16; and column 11, lines 61-65 of MA together, these sections of MA disclose queueing a received packet at an input interface, classification of the received packet to identify its associated priority level that specifies the QoS level that is to be used when handling the

packet, and queuing of the packet in a particular output queue based on the packet's classification. These sections, thus, disclose the retrieval of a received packet from an input queue, where the retrieved packet includes a priority level within the packet, and queueing of the packet in an output queue based on the priority level. These sections of MA, as admitted by the final Office Action, do not disclose, or even suggest, "wherein the memory is configured to be preprogrammed with the plurality of priority levels by a host device," as recited in claim 15.

At paragraph **[0043]**, LEFEBVRE discloses:

> Each of the distinct queue priority determining means in this first variant of the first embodiment then merely consists of a memory register storing the corresponding associated priority value, a detection means for checking the status of the associated storage queue, as well as output means for delivering the appropriate queue priority to the interface module priority means. The detection means checks whether the associated storage queue is empty, upon this condition the associated storage queue or interface module priority is for instance set to 0.

This section of LEFEBVRE discloses a memory register that stores an associated priority value. This section of LEFEBVRE, however, does not disclose or suggest the memory register being *preprogrammed with a plurality of priority levels by a host device*, as recited in claim 15.

In view of the discussion above, the combination of the disclosures of MA and LEFEBVRE disclose the queueing of receiving packets at an input queue, where the received packets include a priority level indicator within each of the packets, retrieval of the packets from the input queue and storing of the packets in output queues that correspond to each of the

packet's priority level indicators, and storing a priority value in a memory register. Neither MA nor LEFEBVRE, either singly or in any reasonable combination, discloses or suggests "a memory configured to store a plurality of priority levels, one for each of the plurality of classes of service, wherein the memory is configured to be preprogrammed with the plurality of priority levels by a host device," as recited in claim 15.

The combination of MA and LEFEBVRE, thus, contrary to the allegations of the final Office Action, does not disclose or suggest the combination of features recited in claim 15. The final Office Action, therefore, has failed to establish a *prima facie* case of obviousness. Reversal of the rejection of claim 15 is, thus, respectfully requested.

VIII. CONCLUSION

For at least the foregoing reasons, it is respectfully requested that the Examiner's rejections of claim 15 under 35 U.S.C. §103(a) be REVERSED.

Respectfully submitted,

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CLAIMS APPENDIX

THE APPEALED CLAIMS

The claim on appeal is as follows:

15. A multiport network device, comprising:

a plurality of input ports configured to receive a plurality of data frames, each of the data frames specifying at least one of a plurality of classes of service;

a plurality of output ports configured to transmit at least some of the data frames;

a plurality of priority queues associated with each of the output ports;

a memory configured to store a plurality of priority levels, one for each of the plurality of classes of service, wherein the memory is configured to be preprogrammed with the plurality of priority levels by a host device;

an action generator including:

an action memory configured to store a plurality of entries,

a decoder configured to identify one of the entries in the action memory for each of the data frames, and

a tag generator configured to generate an action tag based on the entry identified for each of the data frames; and

a port vector queue configured to access the memory to retrieve one of the stored priority

levels that corresponds to a class of service specified by each of the data frames using the action tag from the action generator for the data frame and identify one of the priority queues based on the identified priority level information for the data frame.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None